

A Reduced Intermodulation Distortion Tunable Ferroelectric Capacitor: Architecture and Demonstration

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Abstract — A ferroelectric tunable capacitor device architecture is presented that allows for a reduction of intermodulation distortion (IMD), while maintaining high tunability at low bias voltages. The tunable capacitor is fabricated from epitaxial thin-film barium strontium titanate (BST) deposited on a sapphire substrate. The RF portion of the capacitor is a conventional planar gap capacitor with a 10~14 μ m gap. However, rather than superimposing the DC bias on the RF gap, a separate bias structure is fabricated within the RF gap. The interdigital bias structure has narrowly-spaced high resistance ($2\sim 3 \times 10^4 \Omega/\square$) indium tin oxide (ITO) electrodes spaced 1~2 μ m apart. The high resistivity of the bias electrodes decouples the DC bias from the RF signal path. This bias structure allows high DC fields to be developed with less than 30V applied to tune the material permittivity, but is sufficiently resistive to avoid affecting the Q of the RF capacitor. Because the RF gap is wide, the IMD performance remains good, even at modest tuning voltages. Three different gap capacitors have been fabricated for concept verification: 1) a conventional gap structure (without bias structure), 2) the proposed RF gap capacitor with the DC bias structure, and 3) a narrower conventional RF gap capacitor structure used as an IMD reference. The frequency response of the proposed gap capacitor with the bias structure is characterized and its analysis shows that the highly resistive bias lines are serving as a DC bias path for high tunability, but are not attenuating the RF signal. Two-tone IMD tests show that the IMD performance for the gap capacitor with the bias structure is improved by 6 dB over the conventional reference structure at the same tunability.

I. INTRODUCTION

Barium strontium titanate, $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ (BST), is a very attractive RF tunable material due to its large field-dependent permittivity, high dielectric constant, and relatively low loss tangent. In addition, varactor diodes created from this material have no junction noise compared to semiconductor varactor diodes [1,2]. By using these advantageous properties of BST, a number of advanced high frequency tunable capacitors have been successfully demonstrated and integrated into RF components, such as phase shifters and RF filters [3-6]. One of the fundamental issues affecting tunable capacitors is the inherent intermodulation distortion (IMD) created by the RF field modulating the device capacitance. In a

conventional capacitor, the IMD performance is directly proportional to the tunability of the capacitor, as expressed in equation (1) [7]:

$$\text{IMD} \propto V_{\text{RF}}/V_{\text{DC}} \quad (1)$$

where V_{RF} is the amplitude of the RF signal voltage and V_{DC} is the voltage required for tuning. Based on this relationship, one approach to improve IMD performance in high RF-power handling devices is to make the DC tuning voltage much higher than that of any RF voltage level. While this approach is effective, tuning voltages often exceed 100V. Although no significant current is drawn to bias the capacitor, a systems problem results in supplying the high static potentials required for this approach.

This paper describes a device architecture that addresses the IMD issue by means of a capacitor which has a separate DC bias structure that is constructed within the RF gap capacitor. Figure 1 shows a conceptual sketch of this device structure. The RF capacitor is a conventional

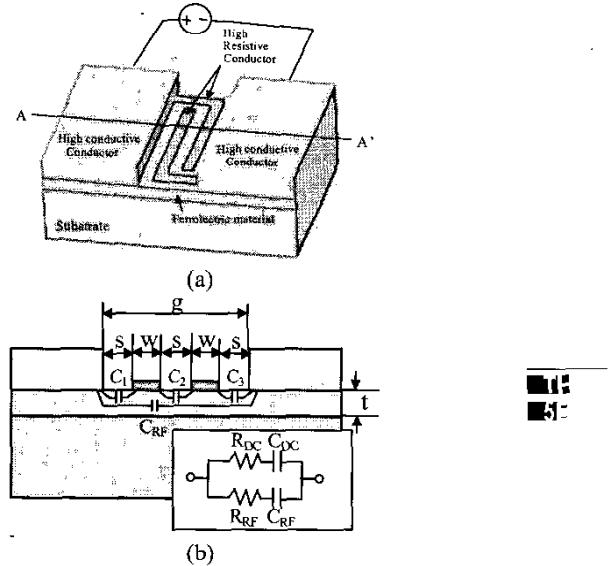


Fig. 1. Schematic of reduced IMD structure; (a) isometric view, (b) cross-sectional view of A-A' (an equivalent circuit is shown in the inset)

microwave gap capacitor that uses high conductivity electrodes to ensure good Q . In contrast, the DC bias structure is fabricated with high resistivity interdigital structures. At low frequencies, such as those used to change the tuning bias voltage, the high resistivity lines present a negligible impedance compared with that of the gap capacitor and the full tuning voltage appears across the lines, changing the permittivity of the structure and therefore the capacitance. However, at signal frequencies, the impedance of the bias lines exceeds that of the gap capacitor itself, so the RF current travels through the (permittivity-tuned) ferroelectric material. Because the RF field is effectively isolated by the high resistance of the bias structure, no degradation in IMD performance occurs. Furthermore, if the resistivity is kept high enough, no noticeable degradation in capacitor Q will occur, since the RF field will preferentially interact with the low-loss, low-impedance BST capacitor.

II. DESIGN AND FABRICATION

A cross-sectional view and its simplified equivalent circuit are shown in Figure 1b and its inset, respectively. In the circuit, the upper branch consists of an equivalent series resistance of the highly resistive conductor line R_{DC} and a capacitance C_{DC} from the integration of C_1 , C_2 , and C_3 . The lower branch has a series resistance of pads R_{RF} and RF capacitance C_{RF} between the highly conductive conductors with a gap g through the ferroelectric layer. We assume the capacitance through the ferroelectric layer is dominant and the capacitance through the substrate and the air may be ignored, due to the relatively high dielectric constant of the ferroelectric material. Therefore, C_{RF} , and the associated Q as determined by R_{RF} , is determined by the geometry of the metal. It is clear that the cutoff frequency of the DC bias structure should be well below the frequency of operation of the tunable capacitor. This implies that R_{DC} should be as high as possible. The only restriction is that the time constant formed by this structure, $\tau_{DC} = R_{DC} C_{DC}$, may limit the rate at which

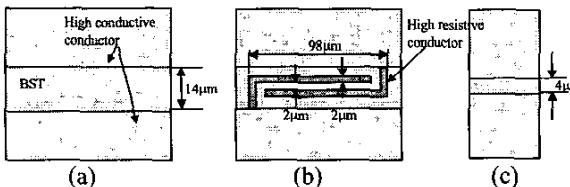


Fig. 2. Gap capacitor configurations for performance comparison (top view); (a) no bias structure (conventional gap capacitor), (b) bias structure (proposed gap capacitor), (c) IMD comparison structure (narrow gap capacitor)

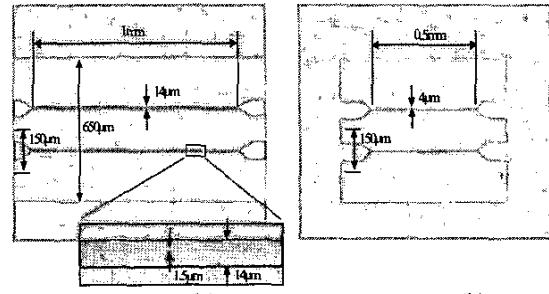


Fig. 3. Photomicrograph of the fabricated gap capacitors; (a) bias configuration (14 μm RF gap, 1.5 μm dc biasing gap, 1mm long, 10 repeated bias structure); magnified unit bias electrodes in the inset (SEM picture) (b) IMD comparison narrow gap capacitor (4 μm gap, 0.5mm long)

tuning may occur. There is also a restriction as to the orientation of the DC field. It was found that the DC field must be parallel with the RF field to insure maximum tunability. This was verified in another structure that had a perpendicular DC field, and showed little RF capacitance change with DC voltage.

To verify the device concept, three test capacitors have been designed, fabricated, and tested: 1) a conventional RF gap capacitor (without a DC bias structure) with a 14 μm gap; 2) the proposed capacitor incorporating the DC bias structure with 2 μm spacing and 2 μm width; and 3) a narrower gap (4 μm) RF structure used as an IMD reference. These structures are illustrated in Figure 2.

Barium strontium titanate ($\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$; BST) ferroelectric thin films (450 nm thick) epitaxially grown on sapphire substrates (430 μm thick) using combustion chemical vapor deposition (CCVD) by Microcoating Technologies, Inc., Chamblee, GA, are used as a starting wafer [8]. For the highly resistive bias structure electrodes, 10 nm thick Indium Tin Oxide (ITO) was deposited using RF sputtering and patterned with lift-off. The measured sheet resistance of the ITO was approximately $2\text{--}3 \times 10^4 \Omega/\square$. Each pair of ITO has 100 μm of overlap. Lastly, the RF conductors were formed using a standard lift-off process with 1 μm thick copper and 0.3 μm gold.

To minimize the parasitic capacitance between signal and ground lines, a shunt capacitor scheme was adopted using the coplanar waveguide configuration. A fabricated device with ten repeated bias structures is shown in Figure 3. Figure 3a shows the bias structure, which has a 14 μm RF gap, a 1.5 μm DC bias gap (smaller gap is obtained after fabrication), 1 mm long electrodes, and 10 repeated unit bias structures; and Figure 3b shows a 4 μm gap and 0.5 mm long IMD reference structure.

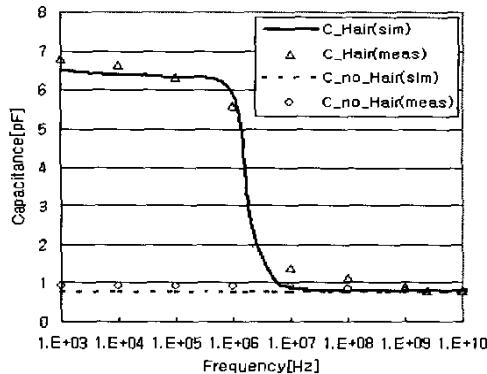


Fig. 4. Capacitance comparison with bias structure and no bias structure according to frequency

III. RF Test Results

A. Frequency Response

In Figure 4, the capacitances of the bias structure and the RF gap capacitor are compared as a function of frequency. In the low frequency region, the capacitance of the bias structure is attributed to the sum of the capacitance from RF electrodes (C_{RF}) and that from high resistive bias electrodes (C_{DC}) (Figure 1b). As the frequency increases, the major impedance of the RF branch due to C_{RF} ($=1/\omega C_{RF}$) becomes smaller while the impedance of the highly resistive bias structure is not changing much due to its smaller frequency dependence (R_{DC}). In the frequency range above 10MHz, the overall impedance of the bias structure is dominated by the RF path, resulting in its convergence to that of the no-bias structure. This result demonstrates that the highly resistive bias line is not functioning as a capacitive component in

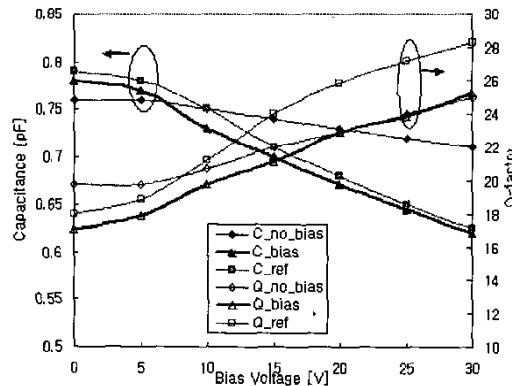


Fig. 5. Q factor and Capacitance as a function of the DC bias voltage at 2.5 GHz.

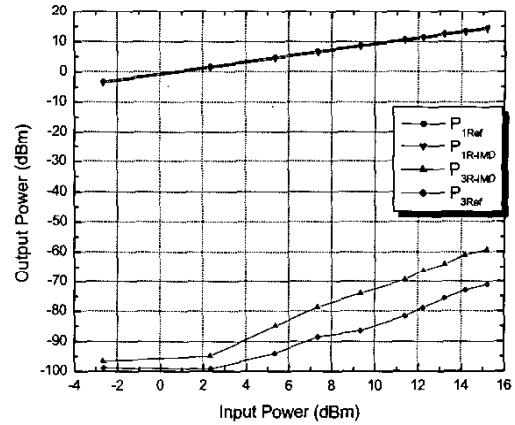


Fig. 6. Fundamental (P_1) and third order intermodulation power (P_3) as a function of input power.

the high frequency regime. Meanwhile, the capacitor of the no bias structure is not dependent on the frequency, as expected.

A circuit simulation is carried out using the simplified circuit in Figure 1b inset to extract lumped parameter values. The simulation result of capacitance is plotted in Figure 4 with solid line and dashed line for the bias structure and no bias structure, respectively. The extracted lumped parameters are summarized in Table 1. The measured capacitance and quality factor as a function of the DC bias voltage at 2.5GHz are shown in Fig. 5. Approximate tunability (C_{max}/C_{min}) of 1.27 (21%) at 30V was obtained both for reduced IMD and reference capacitors, as we expected, while only 1.08 (7%) was obtained for the no bias capacitor. Quality factors for all three structures were over 16 at zero bias voltage. Note that the quality factor of the proposed bias structure was not materially degraded due to the highly resistive bias lines, as expected.

Table 1. Circuit parameters for the bias and no bias structure

	C_{DC}	R_{DC}	C_{RF}	R_{RF}
Bias structure	6.8pF	$10^5\Omega$	0.80pF	5Ω
RF capacitor	0	∞	0.75pF	5Ω

B. IMD Test Results

Two-tone IMD tests were performed for the capacitor with the proposed bias structure (reduced IMD capacitor) and the IMD reference capacitor with 4μm gap. The equal-power input signals are separated by 50 kHz ($f_{RF1} = 2$ GHz, $f_{RF2} = 2.00005$ GHz). A cancellation setup was used in order to keep the noise-floor of the RF signal at a low level, making it possible to measure intermodulation

over a wide range. Figure 6 shows fundamental output

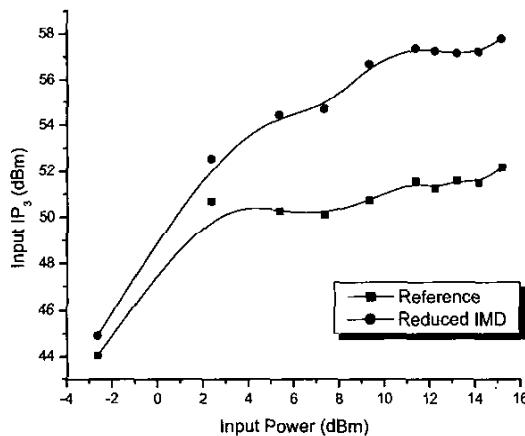


Fig. 7. Input IP₃ versus input power.

power and IMD₃ power of the reference and the reduced IMD capacitors as a function of input power. At the low input power range (below 10 dBm), the third order intermodulation powers (P₃) of both capacitors are close to each other due to the noise-floor of the signal. Beyond 10 dBm, the difference of P₃ is about 12 dB. Input IP₃ (IIP₃) as a function of input power is shown in Figure 7. IIP₃ is calculated by measuring both fundamental and IMD₃ and applying following formula:

$$IIP_3 = OIP_3 - Loss = (P_{1out} + IMD_3 / 2) - Loss \quad (2)$$

Approximately 6 dB improvement of IIP₃ was obtained beyond 10 dBm input power. Compared to the reference structure, we can achieve the same tunability and 6 dB IIP₃ improvement using the reduced IMD capacitor. The high frequency measurements at 2.5GHz are summarized in Table2.

Table 2. Summary of high frequency measurement at 2.5GHz

	No bias structure		Bias structure		IMD reference	
	0V	30V	0V	30V	0V	30V
Capacitance [pF]	0.76	0.71	0.78	0.62	0.78	0.62
Q-factor	19.8	25.0	17.1	25.0	18.0	28.3
Tuning	7%		21%		21%	
IIP3	58dBm		58dBm		52dBm	

V. CONCLUSIONS

A low IMD tunable capacitor architecture with a high resistivity DC bias structure within an RF gap capacitor was designed, fabricated, and tested. The performance of the capacitor with the DC bias structure showed 6 dB better IMD performance when compared with the equivalent conventional gap capacitor design. Both structures showed tunability as 21% at 30V. From frequency response and impedance measurements, it was also concluded that the DC bias structure did not significantly degrade the Q of the capacitor.

VI. ACKNOWLEDGEMENTS

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